

PFR-038 Title: DFB FPGA MD19 discontinuity

Assembly : DFB Component : Originator: Aref Nammari		SubAssembly : DFB SN004 Date: 4/18/05 Organization: LASP					
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Failure Occurre	d During (Check one √ √Qualification test) S/C Integration	□ Launch operations				
Environment wh	en failure occurred:						
× Ambient	□ Vibration						
□ Thermal	□ Vacuum	□ Thermal-Vacuum	\Box EMI/EMC				
	Drobla	m Description					

(In this section it is important to document the specific symptoms that exhibited the problem. In the event we see it happen again, we would like to know as much as possible.)

FFT noise floor too high.

Analyses Performed to Determine Cause

(How do we know how the failure happened? Was it a bad part, bad handling, what?)

It was determined that there was a discontinuity between the data line MD19 and FPGA 2 (U51). Further testing was done to determine where the problem was. It was determined that it could be in one of three places: a broken trace between resistor pad and via, open via or a broken internal trace. Examination under the microscope did not show an obvious break in the trace between resistor pad and via. It was also hard to determine the integrity of via and it is impossible with available tools to determine the integrity of the internal trace. Solder mask should be removed from via pad on both top and bottom layers and continuity measurement should be performed to determine the via integrity.

Corrective Action/ Resolution

(How do we fix the unit? And how do we make sure it doesn't happen again?)

A jumper wire is to be soldered between the memory chip U55 pin 17 and the resistor R234 pad to where the trace should have been connected. Epoxy should cover the area of the board (both top and bottom surfaces) where the solder mask was scraped off to allow for via integrity testing. Because of potential stub hanging at either end signal integrity of MD19 should be evaluated.



Acceptance: MAM: Ron Jackson	_; MSE: Ellen Taylor
PM Peter Harvey	; Cognizant EngineerAref Nammari
Date of Closure	