PFR-029 Title: Solder bridge on FPGA #2 on FM-2

Assembly :	**SubAssembly : DFB SN003**
Component :	
Originator: Ken Stevens	**Organization: LASP**
Phone: (303)449-3887	**Email : ken.stevens@lasp.colorado.edu**

Failure Occurred During (Check one √)

× Functional test □ Qualification test □ S/C Integration □ Launch operations

Environment when failure occurred:

× Ambient □ Vibration □ Shock □ Acoustic
□ Thermal □ Vacuum □ Thermal-Vacuum □ EMI/EMC

Problem Description

(In this section it is important to document the specific symtoms which exhibited the problem. In the event we see it happen again, we would like to know as much as possible.)

During initial testing at LASP, the design seemed to be functioning correctly but was drawing significantly more power than expected.

Analyses Performed to Determine Cause

(How do we know how the failure happened? Was it a bad part, bad handling, what?)

The power dissipation for various modes was initially measured as:

Operation Mode	Current Draw in mA						Total Power
	+2.5VD	+5.0VD	+5.0VA	-5.0VA	+10VA	-10VA	
SS Only	91	258	32	33	7	6	1972 mW
Typical FS	91	261	35	35	7	6	2012 mW
Max Proc	193	305	40	42	7	6	2547 mW

A survey of the parts was performed to determine if any of them were dissipating excess current. Using an informal finger test method, FPGA #2 seemed to be warmer than the other components even though the mode that the DFB was running in did not enable FPGA #2. A thermistor was attached in sequence to each of the FPGAs to determine the temperature of the FPGAs in different modes. The results were:

Operation Mode	Temperature in degrees Celsius		
	FPGA #1	FPGA #2	FPGA #3
Powered Off	25	25	25
Default Mode	31	42.5	25
Derived Ideal Mode	31	45	29

This testing revealed that FPGA #2 was significantly warmer than the others even in the default mode where it is not used and should have been closer to the 25 degrees observed on FPGA #3. A microscopic inspection of FPGA #2 revealed that there was a solder bridge between pin 148 (VCCI) and pin 147 (an unused output driven to ground). After removing the solder bridge, the power was again measured:

Operation Mode	Current Draw in mA						Total Power
	+2.5VD	+5.0VD	+5.0VA	-5.0VA	+10VA	-10VA	
SS Only	91	33	32	33	7	6	847 mW
Typical FS	92	34	33	34	7	6	865 mW
Max Proc	203	90	37	42	7	6	1482 mW

These numbers are in line with the expected values and showed that the FPGA was sinking approximately 1.1 W in excess current through these pins.

Corrective Action/ Resolution

(How do we fix the unit? And how do we make sure it doesn't happen again?)

Replacement of FPGA #2 (U51) is recommended since this part was stressed by a direct power to ground short internal to the part. Future boards should be thoroughly inspected using a microscope prior to power-up.

Acceptance:
MAM: Ron Jackson_____; MSE: Ellen Taylor_____

PM Peter Harvey_____; Cognizant Engineer__Ken Stevens_____

Date of Closure_____