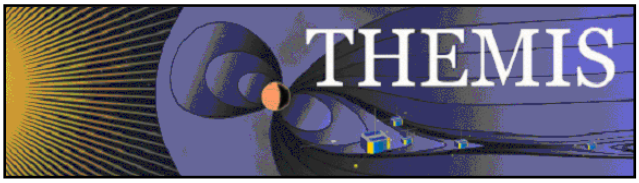



# THEMIS
# Fluxgate Magnetometer (FGM)
# Interface Control Document (ICD)

THM-SYS-106
Oct 21, 2004
Revision F

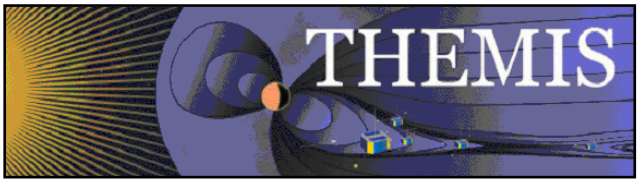
*thm_sys_106F_FGM_ICD*

Ellen Taylor, U.C.Berkeley THEMIS Mission Systems Engineer

Peter Harvey, U.C.Berkeley THEMIS Project Manager

Hans-Ulrich Auster, TU-Braunschweig FGM Technical Manager

Werner Magnes, IWF Graz FGM Co-TM

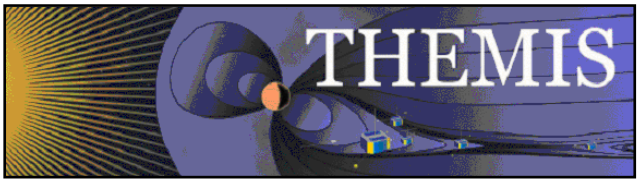



## Distribution List

| Name | Email |
|---|---|
| Hans-Ulrich Auster, FGM TM, TU-BS | uli.auster@tu-bs.de |
| Robert Abiad, ETC Lead, U.C.Berkeley | abiad@ssl.berkeley.edu |
| Peter Berg, LVPS Electronics, UCB | pcb@ssl.berkeley.edu |
| Dorothy Gordon, DCB Electronics, UCB | dag@elfelectronics.com |
| Stu Harris, BEB Electronics, UCB | sharris@ssl.berkeley.edu |
| Frank Harvey, FSW, UCB | fharvey@ssl.berkeley.edu |
| Peter Harvey, Project Manager, UCB | prh@ssl.berkeley.edu |
| Olaf Hillenmaier, FGM, Magson | olaf@magson.de |
| Ronald Kroth, FGM, Magson | ronald@magson.de |
| Jim Lewis, EGSE, UCB | jwl@ssl.berkeley.edu |
| Aref Nammari, DFB Engineering, LASP | aref.nammari@lasp.colorado.edu |
| Werner Magnes, FGE Electronics, IWF | werner.magnes@oeaw.ac.at |
| Ken Stevens, DFB Electronics, LASP | ken.stevens@lasp.colorado.edu |
| Ellen Taylor, Mission Systems, UCB | ertaylor@ssl.berkeley.edu |
| Paul Turin, Mechanical Lead, UCB | pturin@ssl.berkeley.edu |

## TBDs

| Chapter | Description |
|---|---|
| | |
| | |
| | |
| | |



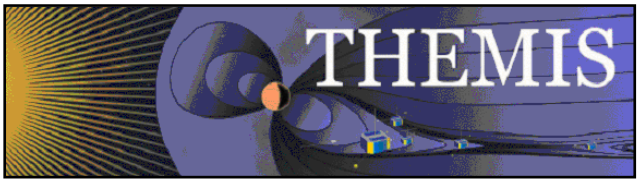

## Revision List (I/F Requirements Document)

| Issue | Rev. | Date | Section | Change |
|---|---|---|---|---|
| Draft | 0 | 12 May 03 | | Document created |
| 1 | 0 | 16 Sep 03 | all | New issue for FGM PDR |
| 1 | 1 | 18 Sep 03 | 5 | FGM commands (Tab. 4.1) |
| 1 | 2 | 02 Oct 03 | 5.1 | command synchronization with 25 zeros |
| | | | 2 | TML: command able between 4 Hz and 128 Hz |
| 1 | 3 | 30. Oct 03 | 5-8 | Chapter order corrected |
| | | | all | Table and figure number format changed |
| | | | 3 | Centred 128 Hz data |
| | | | 4.1 | Tab. 4.1: Control word bit order changed |
| | | | 4.2 | Status bit definition |
| | | | 6 | Update of FGM voltages |
| | | | 8 | FGS sensor harness |

## Document Revision Record (FGM ICD)

| Rev. | Date | Description of Change | Approved By |
|---|---|---|---|
| C | 17 Nov 03 | Ch 4.1: FGM sub-command | - |
| | | Ch 8: Tab. 8.1 Connector description | |
| | | Ch 8: Harness mass estimate | |
| | | Ch 2: FPGA 1/2 description deleted (instead FPGA SE and FPGA IF) | |
| | | Ch 2: Block diagram updated | |
| | | Tab. 4.1: Filter modes included | |
| | | Tab. 4.4: Filter mode status bits | |
| D | 08 Apr 04 | Ch 8 Grounding at FGM sensor | |
| | | Fig. 8.3 update of harness length | |
| | | Tab. 8.3 updated | |
| | | Tab. 4.1 FGM Control word:<br>Bit 2/1: standard and three calibration modes;<br>Bit 9: Synch. to FGE internal 1 sec pulse<br>Bit 10: Excitation on/off;<br>Filter mode 3 is default mode; | |
| | | Tab. 4.1: classification of signed and unsigned command parameters | |
| | | Tab. 4.1 additional command: 0x8C Kf factor | |
| | | Tab 4.4 status bits:<br>only one feedback relais status bit;<br>status bit in case of synchronization to FGE internal 1 sec pulse; | |
| | 14 May 04 | Tab. 4.1 FGM Control word bit 9 *synchronization internal / extern* removed | |
| E | 26 May 04 | Tab. 4.4 status bits:<br>status bit 4 *synchronization to FGE internal 1 sec pulse* removed; feed back relais status is bit 4; bit 2 and 3 show status of instrument mode | |
| | | Ch 5 H/K temperature transfer function included | |
| | | Ch 8 FGS boom harness length of 96'' | |
| | | Ch 5 Reference to THM-SYS-005 included | |
| | | Ch 4.2 DCB samples on the next rising edge of CLK | |
| F | 16 Aug. 04 | Tab. 8.2: New Gore cable for feedback signals | |

| | | | |
|---|---|---|---|
| | 04 Oct. 04 | Tab. 4.1: # of Phase bits is 0+8 instead of 0+16 | |
| | | Tab. 4.1: # of Sampling bits is 0+6 instead of 0+16 | |
| | | Tab. 4.1 and 4.3: # of DACxyz2 bits is 4+6 instead of 4+12 | |
| | | Ch. 4.2: instrument ID included to Y-MSB (Tab. 4.5) | |
| | | Ch. 2: the dyn. range is 25,000 nT with 2.98 pT res. | |
| | | Ch. 7, Fig. 7.3: unit axes of FGS not identical with magnetic axes. | |
| | | Ch. 3: timing accuracy of the centered TMH data as well as the averaged TML data included | |
| | | Tab. 6.1: Update of the supply currents according to FGE6/FGS6 measurements | |
| | | Ch. 4.1 FGM turn-on: No default values in FPGA | |
| | 21 Oct. 04 | Ch. 4.1 A command with parity and/or stop bit error is executed by FGE but it is reported in the status information. | |
| | | Tab. 4.1: CAL mode 2 control bit included (bit 12 of Control Word) | |




# 1. Introduction

This document describes the electrical and mechanical interfaces between the Fluxgate Magnetometer and the IDPU Power Control Board (PCB), the IDPU Data Control Board (DCB) as well as the magnetometer boom.
Until Nov. 17, 2003, this document was handled as FGM Interface Requirements Document. The final version, before its conversion to the official Themis Interface Control Data (ICD) standard, was issue 1 and revision 3 (see revision list).
The FGM ICD document starts with revision C.

# 2. FGM Operation Principle

FGM operates as a digital fluxgate magnetometer (block diagram in figure 2.1).
The sensor electronics generates an excitation AC current (drive/excitation frequency at 8192 Hz, F0), which drives the soft magnetic core material of the two ringcores deep into positive and negative saturation. The external magnetic field distorts the symmetry of the magnetic flux and generates field proportional even harmonics of the drive frequency in the sense coils.
The induced voltage in the sense coil is digitized after the preamplifier (14-bit ADCs from Maxwell) at four times the driving frequency (4F0). The accumulation of multiples of four consecutive data samples is necessary in order to cancel out all odd harmonics of the excitation signal, which couple from drive to sense inductively.
One 54SX72 FPGA is used for generating all needed control and interface singles as well as for the FGM internal data processing. For a better understanding of the FGM operation principle, the FPGA is internally split into a near sensor electronics (FPGA SE) and a digital interface part (FPGA IF) in the block diagram of figure 2.1.
The 'front end' signal processing (synchronous detection and integration of the sense signal and calculation of the feedback values) is done by FPGA SE. In order to increase the overall linearity and stability of the magnetometer a feedback field has to be supplied to the sensor by using two cascaded 12-bit DACs and a separate pair of feedback coils (Helmholtz coils) per sensor axis. Sense and feedback signals are continuously transmitted to the FPGA IF part of the Gate Array (128 Hz) which calculates the magnetic field values by scaling and adding up the received data (k1*ADC+k2*DAC). Additionally, FPGA SE averages the data for the low (4, 8, 16, 32 and 64 Hz) telemetry output (TML), calibrates the magnetic field data (only offset) and handles the serial interface to the IDPU.
The digital concept requires analog-to-digital conversion at a higher data rate but it shows a number of advantages over the traditional analog fluxgate magnetometer. The early digitization makes the sensed signal e.g. much more robust to changes of the environmental temperature and the supply voltage as well as insensitive to electro-magnetic interference which is important for the common E-box and shared board design. Furthermore, no range switching is needed for getting a ±25,000 nT dynamic range in parallel with 2.98 pT resolution, which is equivalent to a 24-bit digital-to-analog conversion.
In standard mode, FGM transmits magnetic field vectors (24 bit per axis) with 128 Hz using the high resolution and an averaged number of vectors using the low resolution telemetry line.
In calibration mode the FPGA SE doesn't calculate the feedback values (set from IDPU per command) and only the ADC mean values (24 bit per axis) are transmitted. A hidden calibration mode exists when setting either k1 or k2 to zero in standard mode.

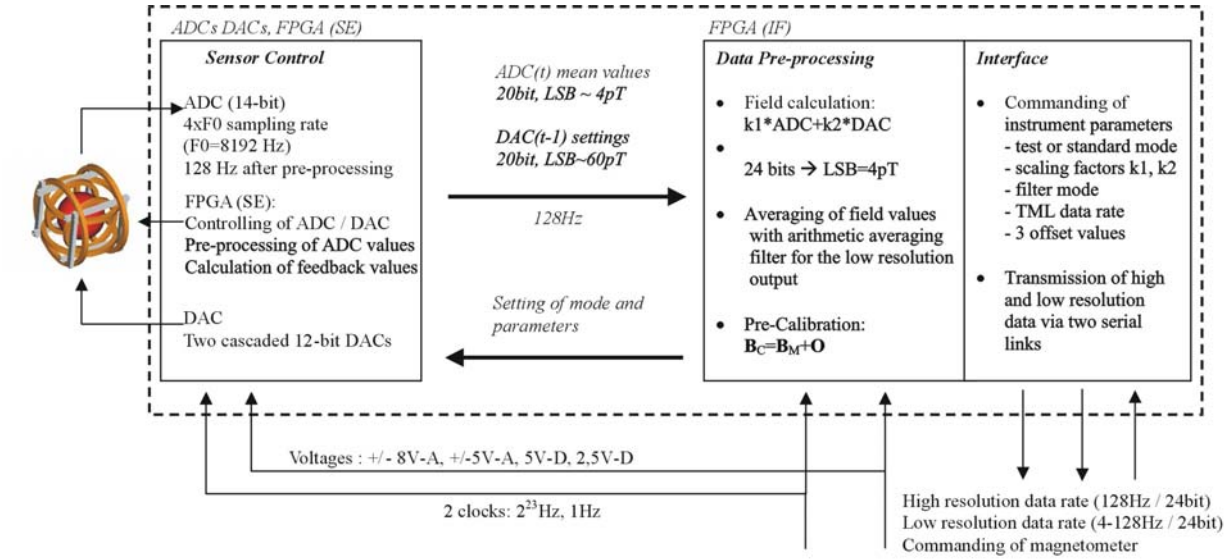



*Fig. 2.1 FGM block diagram*

## 3. High Resolution Clock and Timing

Due to the measurement principle of the digital magnetometer mentioned in the previous section the excitation frequency F0 must be an integral multiple (N1) of the maximum output data rate (proposed 128 Hz) as well as the high resolution clock used by FGM must be an integral multiple (N2) of F0. Whereas N2 should ideally be a power of two.

$$Clk=N2*N1*128 \qquad (1)$$

With the high resolution as well as serial interface clock of 2^23 Hz, CLK8MHz, proposed for Themis, N1 will be 64 and N2 is equal to 1024. The excitation frequency F0 will be 8192 Hz.

The 128 Hz output vectors (TMH and TML) are centered mean values relative to the 1 Hz synchronization clock (CLK1Hz). This means, that every 128$^{th}$ output vector (X, Y and Z) is exactly measured over the CLK1Hz tick with a guaranteed accuracy of 250 us (see figure 3.1).

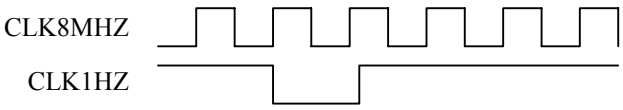



*Fig. 3.1 1 Hz clock (CLK1Hz) synchronization*

The vector following the centered vector is the one which is transmitted first after the magnetic field sampling has been start by setting the start bit in the control register by command. This vector is also the one with which the averaging of the TML output data is started.
The timing relative to the CLK1HZ tick of the first TML vector transmitted after the CLK1HZ tick with respect to filter mode and data decimation is depicted in the following table.

| Filter Mode | Output Data Rate | Timing [msec] | Filter Mode | Output Data Rate | Timing [msec] | Filter Mode | Output Data Rate | Timing [msec] |
|---|---|---|---|---|---|---|---|---|
| 1 | 64 | <0.25 | 2 | 64 | -3.91 | 3 | 64 | -3.91 |
| 1 | 32 | <0.25 | 2 | 32 | -11.72 | 3 | 32 | -11.72 |
| 1 | 16 | <0.25 | 2 | 16 | -27.34 | 3 | 16 | -27.34 |
| 1 | 8 | <0.25 | 2 | 8 | -27.34 | 3 | 8 | -58.59 |
| 1 | 4 | <0.25 | 2 | 4 | -27.34 | 3 | 4 | -121.09 |

*Tab. 3.1 Timing of the TML vector transmitted after the 1 Hz tick relative to this tick*

The frequency characteristics of these 128 Hz output data is that of a single arithmetic averaging filter with no overlapping. The amplitude response shows notches at integral multiples of 128 Hz and the group delay relative to the 1 Hz Clock definition in figure 3.1 is zero.

# 4. Serial Interface Circuit

The serial interface circuit between FGM and IDPU (four-wire serial digital interface with CLK, CMD, TMH and TML) can be realized in full accordance with the interface defined in the Themis IDPU Backplane specification. The interface is used to send command and control information from the IDPU to the instruments, and for the instruments to send data and status to the IDPU.

## *4.1 Command Interface*

Figure 4.1 shows the command interface timing.

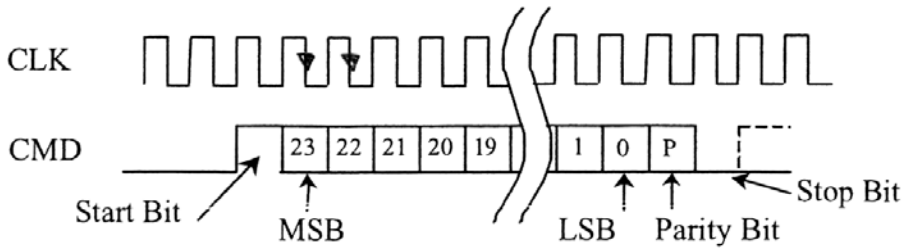



*Fig. 4.1 Serial Command Timing*

### Data Stream Format

Commands are 24-bits long, preceded by a start bit, and followed by parity bit and stop bit. The 24 bits are sent MSB first. The parity is odd and includes the 24 command bits but not the start bit, so that a command with all 24 bits zero would have a parity bit on. Commands can start on rising edge of CLK, and any number of idle bit periods can occur between commands. The data is transferred Most Significant Bit (MSB) first. Messages consist of an 8-bit identifier (CMD_ID) in the 8 MSB (4 bit MSB address and 4 bit LSB unique command-set), followed by a 16-bit data field in the LSB (CMD_DATA).
The parity bit shall be set such that the sum of the number of set bits in the 24 command data bits plus the parity bit is odd. A command with parity and/or stop bit error is executed by FGE – FGM cannot be harmed by any command - but it is reported in the status information.

### FGM Commands

In the current proposal FGM needs 13 commands (4 bits in the command header) with some sub-commands. All sub-commands are coded within the 16-bit data word.

The I+C number in the column '# of Bits' below shows the number of bits for sub-command identification as well as the number of command information bits per command/sub-command.
Commands for sending matrix-elements were defined in earlier versions of this document. Those were deleted.
The FGE command address is 0x8. The command identifier for sending a control word to FGM is therefore 0x81 (see also table 4.2).
The control word defines the operating status of FGM:
Bits 1 and 2 define the principle operating mode of FGM. In standard mode, magnetic field data with 24 bit and 4 pT resolution are transmitted via TMH and TML. In calibration mode 1, the FGE internal feedback values are set to zero (quasi open loop mode) and only the accumulated and filtered ADC values are transmitted. In calibration mode 2, a step function is produced by the FGE digital-to-analog converters for an internal FGM health check (open loop mode). The CAL mode 2 control bit 12 determines whether the complete DAC range or a limited range (about +/- 2000 nT) is applied via the DACs.
In calibration mode 3; the ADC and DAC raw data values are transmitted with 128 Hz via the TMH and TML interface, respectively (closed loop mode).
Bits 4-6 of the control word set the data rate of the TML output. The default data rate after power-on and reset is 4 Hz. The filter mode for the TML output is set with the control bits 7 and 8. In filter mode 1 the TML data are produced by a pure data decimation of the 128 Hz raw data. In filter mode 2, the output data from 16 Hz up to 64 Hz are generated by filtering the raw data with a non-overlapping arithmetic averaging filter (box car). The 4 and 8 Hz output data are gained by a pure data decimation of the 16 Hz data. Finally in filter mode 3, which is also the default filter mode after power-on and reset, all output data rates are calculated by filtering the raw data with a non-overlapping arithmetic averaging filter.

| CMD_ID | Command | # of Bits (I+C) | Remark | |
|---|---|---|---|---|
| 0x81 | Control Word | 0+9 | Bit 0: 1/0 | Start / Stop |
| | | | Bit 2/1: 00<br>Bit 2/1: 01<br>Bit 2/1: 10<br>Bit 2/1: 11 | Standard<br>Calibration mode 1 (open loop)<br>Cal. mode 2 (step function)<br>Cal. mode 3 (AD via TMH and DA via TML) |
| | | | Bit 3: 1/0 | Feedback Relais on / off |
| | | | Bit 6-4: 000<br>Bit 6-4: 001<br>Bit 6-4: 010<br>Bit 6-4: 011<br>Bit 6-4: 100<br>Bit 6-4: 101 | 4 Hz (TML data rate)<br>8 Hz (TML data rate)<br>16 Hz (TML data rate)<br>32 Hz (TML data rate)<br>64 Hz (TML data rate)<br>128 Hz (TML data rate) |
| | | | Bit 8/7: 00<br>Bit 8/7: 01<br>Bit 8/7: 10 | Filter mode 1<br>Filter mode 2<br>Filter mode 3 |
| | | | Bit 9: 1/0 | spare |
| | | | Bit 10: 1/0 | Excitation on/off |
| | | | Bit 11: spare | |
| | | | Bit 12: 1/0 | CAL 2 mode: reduced / full range |
| | | | Bit 15-13 | spare |
| 0x82 | Phase | 0+8 (unsigned) | Phase (limited to 4 … 255d)*) | |
| 0x83 | Sampling | 0+6 (unsigned) | Number of sampling periods M in FPGA SE | |

| | | | |
|---|---|---|---|
| | | | (limited to 1 … 60d) *) |
| 0x84 | K1x | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x85 | K1y | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x86 | K1z | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x87 | K2x | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x88 | K2y | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x89 | K2z | 0+16 (unsigned) | Field calculation in FPGA IF (see figure 2.1) |
| 0x8A | DACx1 | 4+12 (signed) | Setting of DACx1 in calibration mode |
| 0x8A | DACy1 | 4+12 (signed) | Setting of DACy1 in calibration mode |
| 0x8A | DACz1 | 4+12 (signed) | Setting of DACz1 in calibration mode |
| 0x8A | DACx2 | 4+6 (signed) | Setting of DACx2 in cal. mode (dec 0…63) *) |
| 0x8A | DACy2 | 4+6 (signed) | Setting of DACy2 in cal. mode (dec 0…63) *) |
| 0x8A | DACz2 | 4+6 (signed) | Setting of DACz2 in cal. mode (dec 0…63) *) |
| 0x8B | Offset X | 2+14 (signed) | Offset for B calibration |
| 0x8B | Offset Y | 2+14 (signed) | Offset for B calibration |
| 0x8B | Offset Z | 2+14 (signed) | Offset for B calibration |
| 0x8C | Kf | 16 (unsigned) | FGE internal feedback factor |
| 0x8D | | | spare |
| 0x8E | | | spare |
| 0x8F | Reset | 0+0 | Reset |

*Tab. 4.1 FGM commands*

*) Commanding of data which is out of the defined range is ignored by the FGE FPGA.

| Command | CMD_ID [hex] | | Command Data Field [hex] | | | |
|---|---|---|---|---|---|---|
| | **C23-C20** | **C19-C16** | **C15-C12** | **C11-C8** | **C7-C4** | **C3-C0** |
| Start: Control word: Start / Stand. / Exc. on / Rel. on / 32 Hz / FiltM 2 | 8 | 1 | 0 | 8 | B | 1 |
| Reset | 8 | F | x | x | x | x |

*Tab. 4.2 Examples for FGM commands*

The FGM sub-commands (SUB_CMD) for DAC (4 bits) and Offset (2 bits) are defined as follows (see table 4.3). The values are given in binary format.

| CMD_ID | SUB_CMD | Command | # of Bits | Remark |
|---|---|---|---|---|
| 0x8A | 0001 | DACx1 | 12 | Setting of DACx1 in calibration mode |
| 0x8A | 0010 | DACy1 | 12 | Setting of DACy1 in calibration mode |
| 0x8A | 0011 | DACz1 | 12 | Setting of DACz1 in calibration mode |
| 0x8A | 0100 | DACx2 | 6 | Setting of DACx2 in calibration mode |
| 0x8A | 0101 | DACy2 | 6 | Setting of DACy2 in calibration mode |
| 0x8A | 0110 | DACz2 | 6 | Setting of DACz2 in calibration mode |
| 0x8B | 01 | Offset X | 14 | Offset for B calibration |
| 0x8B | 10 | Offset Y | 14 | Offset for B calibration |
| 0x8B | 11 | Offset Z | 14 | Offset for B calibration |

*Tab. 4.3 FGM sub-commands*

## FGM Turn-on

After every turn-on, FGM needs a sequence of commands (phase, sampling, k-factors, offsets and control word, see table 4.2) for a proper operation. There are no default values pre-stored in the FPGA.

### Clocking Edge

The receiving circuit should clock the data bits on the falling edge of CLK (to avoid a race between the CMD and CLK signals). All signal polarities are understood as measured on the back plane.

### Command Synchronization

FGE synchronizes by finding the first non-zero bit (the START bit), and verifies synchronization by the presence of a zero-value STOP bit. After a reset or loss of synchronization, the FGE will look for 25 consecutive zero-level bits before starting to look for a start bit to avoid incorrect interpretation of a transfer in progress.

### Reset Command

FGM shall receive the Reset Command as an instrument specific command with CMD_ID = 0x8F. It is used to stop the FGM data acquisition and to reset the FGM hardware to its default configuration.

### Sample Clock Message

No Sample Clock Messages will be received by FGM. FGM shall produce magnetic field data with a constant delay between data acquisition after the pre-amplifier and data transmission to the IDPU (or DCB, respectively). The link to the sun pulse and the absolute (S/C) time is realized by the IDPU (DCB). See also chapter 3 for centred mean values relative to CLK1Hz produced by FGM

## *4.2 Telemetry Interface*

Figure 4.2 shows the telemetry interface timing.

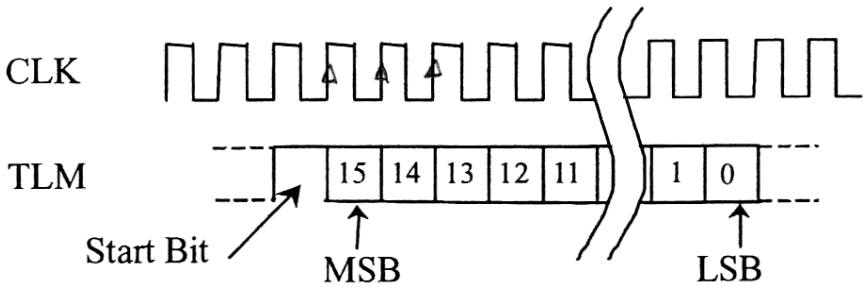



*Fig. 4.2 Serial Telemetry Timing*

### FGM Message

In standard as well as calibration mode, FGM transmits magnetic field vectors (3 24-bit per vector) with 128 Hz using the high resolution and an averaged number of vectors using the low resolution telemetry line. Each 24-bit word is ‘divided’ into two 16-bit words (sign extended). The transmission sequence will be X-MSW, X-LSW, Y-MSW, Y-LSW, Z-MSW and Z-LSW. No message header is foreseen but FGE will transmit 8 bit of status information as well as the instrument ID with every 128 Hz message package of the TMH data stream. The status information is included to the 8 MSBs of X-MSW and the instrument ID is included to parts of the 8 MSBs of Y-MSW (the four MSBs are zero followed by the four ID bits; see Tab. 4.5). Thus, there is no sign extension for the X-MSW and Y-MSW word of the TMH data.

| Status Bit | X-MSW Bit | Status Bit High |
|---|---|---|
| 0 | 8 | Command parity bit error |
| 1 | 9 | Command stop bit error |
| 2 | 10 | Instrument mode bit 0 (bit 1 of control word) |
| 3 | 11 | Instrument mode bit 1 (bit 2 of control word) |
| 4 | 12 | Feedback relais X/Y/Z open |
| 5 | 13 | spare |
| 6 | 14 | Filter mode LSB (bit 7 of control word) |
| 7 | 15 | Filter mode MSB (bit 8 of control word) |

*Tab. 4.4 FGM Status Bits*

| 102 | 101 | 100 | 99 | 98 | 97 | 96 | 95 | 94 | 93 …86 | 85 | 84 … 69 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Start Bit | FM[1] | FM[0] | - | FB | IM[1] | IM[0] | SE | PE | X[23:16] | Start Bit | X[15:0] |
| 68 | 67 … 64 | | | | 63 … 60 | | | | 59 … 52 | 51 | 50 … 35 |
| Start Bit | "0000" | | | | Board_ID | | | | Y[23:16] | Start Bit | Y[15:0] |
| 34 | 33 … 26 | | | | | | | | 25 …18 | 17 | 16…1 |
| Start Bit | sign extension Z | | | | | | | | Z[23:16] | Start Bit | Z[15:0] |
| 0 | | | | | | | | | | | |
| Stop Bit | | | | | | | | | | | |

*Tab. 4.5 TMH bit stream*

### Clock Edge

The instrument shall shift the next bit of the message out on the rinsing edge of CLK. The bit will be sampled by the DCB on the next rising edge of CLK.

### Synchronization

Messages are preceded by at least 17 bits of zeros. The IDPU shall synchronize to the first non-zero bit as the Start bit of the first word of the message. The end of the message should be indicated by a zero where the next start bit should be, followed by at least 16 more zeros. The number of zeros between the messages shall by any number greater than or equal to 17. On reset, or in the event of a failure in the synchronization timing, the IDPU shall abort the message and ignore the data until at least 17 bit zeros in a row have been sent.

### Data Stream Format

Messages shall consist of a block of six 16-bit words sent consecutively without gap (X-MSW, X-LSW, Y-MSW, Y-LSW, Z-MSW and Z-LSW), other than the START bit at the beginning of each word. The data is transferred Most Significant Bit (MSB) first.

## 5. Analog Housekeeping Data and Temperature Limits

The FGM housekeeping analog lines (2), i.e. sensor and electronics temperature, will be passed down the back plane and converted by a central mux-ADC. The buffered voltage range is +/-2.5 V. The exact transfer function from voltage to temperature is: T[°C]= -40[°C/V]*$V_{HK}$[V]. Thus the maximum measurable temperature range is +/- 100 °C.
FGM will be tested according to the temperature limit specifications in THM-SYS-005 (Instrument Payload Verification Plan and Environmental Test Specification).

# 6. Power Supply

The FGM supply voltages with current, ripple and stability requirements are given in table 6.1.
The only really important voltage in terms of accuracy and stability is the +8 VA, since this voltage is used for generating the excitation currents. Its drift has a direct influence on the stability of the sensor offsets.

| Voltage [V] | Current (max) [mA] | Accuracy [%] | Ripple [mVpp] | Stability [%/°C] |
|---|---|---|---|---|
| +2.5 VD | ~~10~~ 70 | +/-5 | 10 | 0.2 |
| +5 VD | ~~10~~ 7 | +/-5 | 10 | 0.2 |
| +8 VA | ~~40~~ 45 | +/-1 | 10 | 0.1 |
| -8 VA | ~~10~~ 18 | +/-5 | 10 | 0.2 |
| +5 VA | ~~15~~ 21 | +/-5 | 10 | 0.1 |
| -5 VA | ~~15~~ 14 | +/-5 | 10 | 0.1 |

*Tab. 6.1 FGM voltages*

# 7. FGS Mechanical Interface

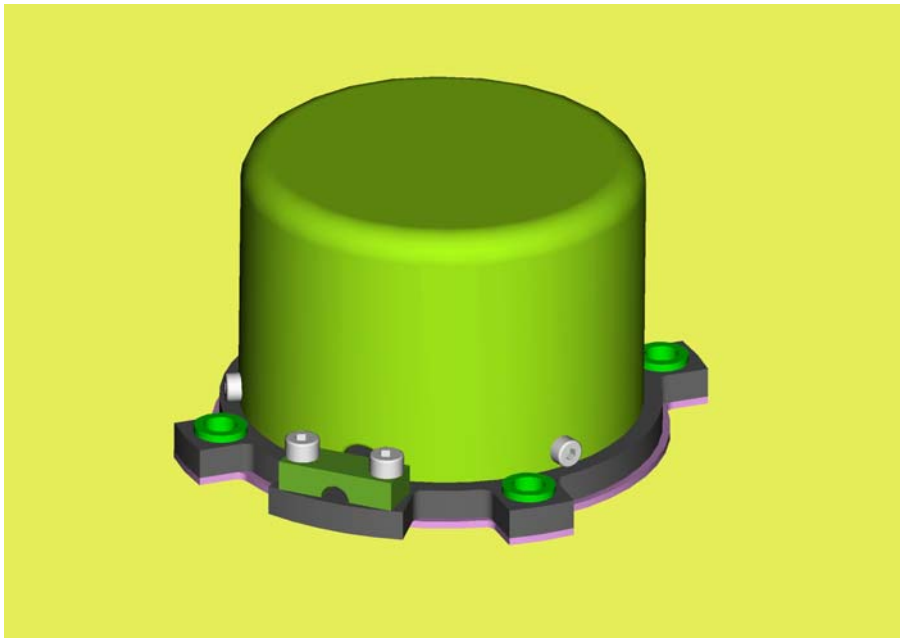


*Fig. 7.1 FGS sensor housing*

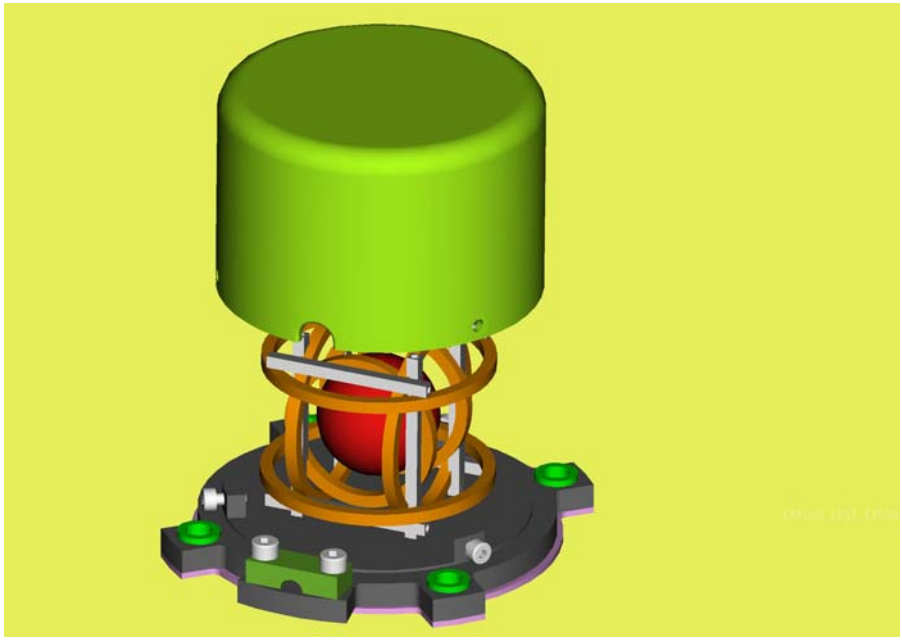


*Fig. 7.2 FGS sensor*

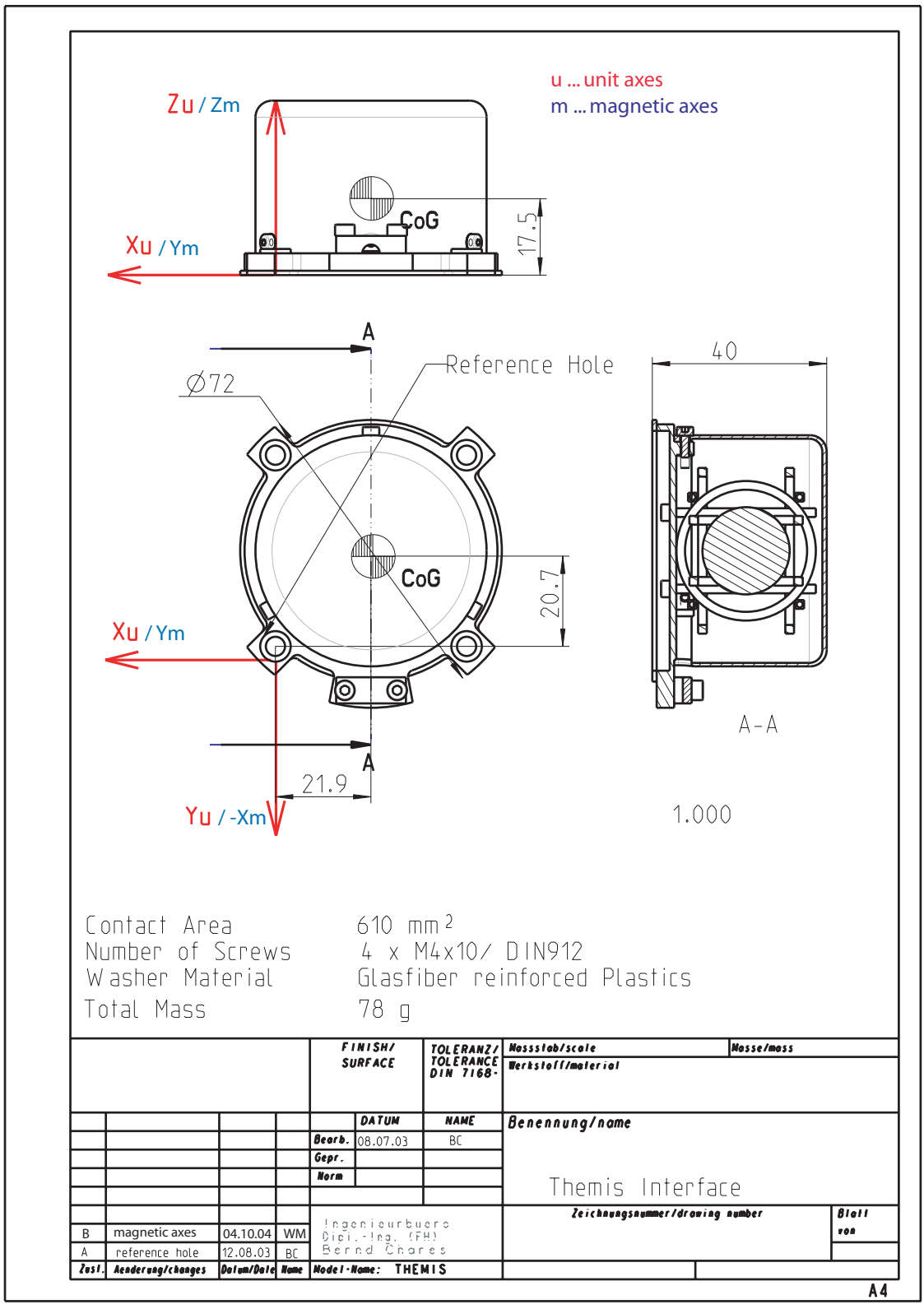



*Fig. 7.3 FGS mechanical interface drawing*

The magnetic axes of the FGSE sensor are not identical with the unit axes as shown in the figure above: Xm = -Yu, Ym = Xu and Zm=Zu!

# 8. FGS Harness

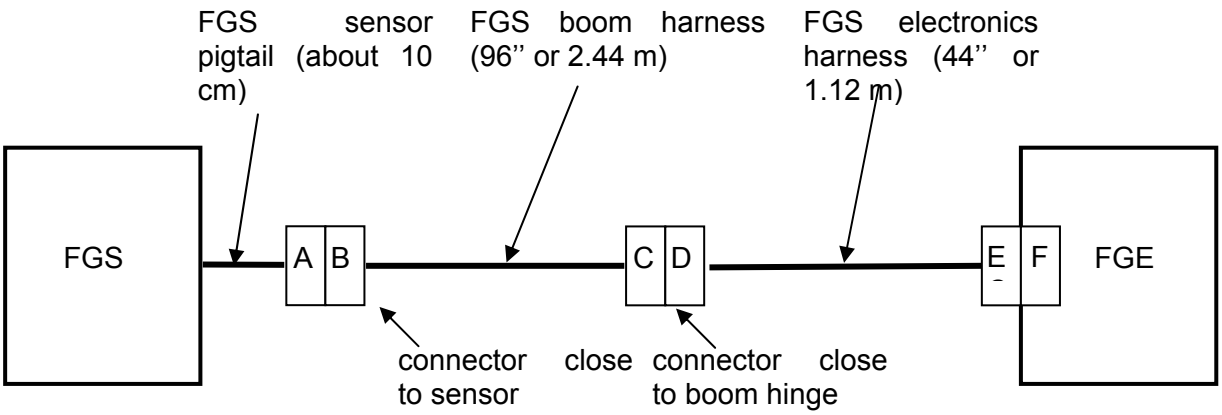



*Fig. 8.3 Block diagram of FGM sensor harness*

For a simplified integration process of the FGM sensor, especially during the tests at Swales, an additional connector pair (with connector bracket on the boom) was added close to the FGM sensor.
An overall shielding with a braided sleeve is foreseen for the complete sensor harness except the sensor pigtail. The connection of the overall shield to the S/C ground (chassis) must be guaranteed via the connector back shells and brackets at the IDPU E-box. The pigtail harness part doesn't need a braided sleeve because it is covered with MLI. The sensor Aluminum housing is connected to pin 11 of the sensor connector and routed along the sensor harness to the PCB/FGE board. There, the Pin 11 is connected to secondary ground which is ultimately routed back to the S/C Single Point Ground (SPG).
The sensor housing will be mechanically isolated from the boom. The inner layer of MLI will be insulating, the outer layer of MLI will be conductive to the boom.
An overview of the FGS harness mass distribution is given in Table 8.3.

| ID of Connectors | Connector Description | Male/Female | Connector Type |
|---|---|---|---|
| A | FGS – pigtail | male | HD-D-SUB 26 P |
| B | boom bracket | female | HD-D-SUB 26 S |
| C | hinge bracket | male | HD-D-SUB 26 P |
| D | hinge bracket | female | HD-D-SUB 26 S |
| E | E-box harness | male | HD-D-SUB 26 P |
| F | E-box FGE board | female | HD-D-SUB 26 S |

*Tab. 8.1 FGM list of connectors*

| Pin | Signal | Type | AWG |
|---|---|---|---|
| 1 | excitation 1 | twisted with 19 and shielded | 28 |
| 2 | temperature | twisted with 20 | 30 |
| 3 | NC | | |
| 4 | feedback Z+[1)] | twisted with 21 | 28 |
| 5 | feedback Y+[1)] | twisted with 22 | 28 |
| 6 | feedback X+[1)] | twisted with 23 | 28 |
| 7 | sense Z+ | twisted with 24 | 30 |

| | | | |
|---|---|---|---|
| 8 | sense Y+ | twisted with 25 | 30 |
| 9 | sense X+ | twisted with 26 | 30 |
| 10 | excitation screen/shield | screen for 1 and 19 | 26 |
| 11 | ground FGS housing | single wire | 26 |
| 12 | feedback screen/shield | screen for 4/5/6 and 21/22/23 | |
| 13-18 | NC | | |
| 19 | excitation 2 | twisted with 1 and shielded | 28 |
| 20 | temperature gnd | twisted with 2 | 30 |
| 21 | feedback Z-[1)] | twisted with 4 | 30 |
| 22 | feedback Y-[1)] | twisted with 5 | 28 |
| 23 | feedback X-[1)] | twisted with 6 | 28 |
| 24 | sense Z- | twisted with 7 | 28 |
| 25 | sense Y- | twisted with 8 | 30 |
| 26 | sense X- | twisted with 9 | 30 |

*Tab. 8.2 FGS pin allocation*

[1)] The 3 x TP with common shield cable from Gore (GSC-05-80499-00) is used for the feedback signals.

| **Device** | **Pcs. / Length (m)** | | | **Mass (g)** |
|---|---|---|---|---|
| | pigtail | boom | electronics | |
| Connector male (11 g) | 1 | 1 | 1 | 33 |
| Connector female (12 g) | 1 | 1 | 1 | 36 |
| Backshell self-made (2 g) | 2 | 2 | 2 | 12 |
| Harness with overall shield (55 g/m) | - | - | 1.12 | 62 |
| Harness without overall shield (30 g/m) | 0.1 | 2.44 | - | 76.2 |
| | | | | |
| | **Total:** | | | **219.2** |

*Tab. 8.3 FGM harness mass*