THEMIS
Digital Fields Board Interface Control Document

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Document Revision Record

Rev.	Date	Description of Change	Approved By
-	9/9/03	Initial Release	-
A	10/16/03	Revised for EFI Peer Review	
B	11/5/03	Revised for formal Release	
C	2/16/04	1. App C Backplane Pin Assignment and Sec. 3.2 SCM Interface: Removed redundant SCM Calibration Signal. (Backplane B25 and Pin 8 DFB/SCM 15-pin SCM_CALINH). This pin will become a DCB I/O Spare on the Backplane. 2. Section 6.6 FGE Data: FGE Data is clocked out on the rising edge from DCB, clocked in on the falling edge at DFB.	
D	3/30/04	1. App C Board Layout Drawing 2. Tsetup and Thold Figure 4, DAG e-mail 3/17/04	
E	5/21/04	Updated Appendix Command and Telemetry List Updated SCM connector (D-Sub Standard) Updated App C Drawing to call out connector Tsetup and Thold Figure 5 same delay as Figure 4	

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TBD List

Identifier	Description

1. Purpose

This document describes the DFB interface to the Data and Controller Board (DCB), Low Voltage Power Supply (LVPS), the Electric Fields Instrument (EFI), the Search Coil Magnetometer (SCM), the Flux Gate Electronics (FGE), and the Power Conditioning Board (PCB). It is intended to document those interfaces so that the various subsystem components can be designed and fabricated based on clear understanding of the requirements.

2. Definitions and Acronyms

DFB – Digital Fields Board
EFI – Electric Fields Instrument
SCM – Search Coil Magnetometer
FGE – Flux Gate Electronics
DCB – Data Controller Board
PCB – Power Conditioning Board
LVPS – Low Voltage Power Supply
EFI_TLM – Telemetry Serial Communication Line
EFI_CMD – Command Serial Communication Line

3. Introduction

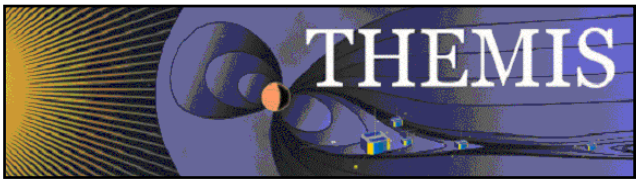
The DFB receives analog signals from the EFI, SCM, and digital data from the FGE instruments. Analog signals are conditioned and converted to digital format. The FGE data is used for Spin Fit data. Data from the DFB is transmitted serially to the DCB. The DFB receives commands from the DCB. The LVPS provides the necessary power to the DFB.

3.1. EFI interface

The DFB-EFI interface shall be through the DFB front panel. The DFB accepts six analog signals from the EFI through six SMA connectors. The amplitude of the EFI signals is in the range of +/- 100V.

3.2. SCM interface

The DFB-SCM interface shall be through one 15 pin standard-D connector on the front panel. Power, +/- 10VDC, shall be routed from the PCB to the SCM through the DFB. Additionally, one digital control signal shall be routed to the SCM from the



DCB through the DFB. The three analog signals provided by the SCM shall have amplitude in the range of +/- 5V (DFB is capable of handling +/-10V inputs). Power and control signals are routed to the DFB from the PCB and DCB respectively through the backplane connector.

Signal	Pin No.	Type	Direction
SCM_P10V	1	+10VDC Power	Out
SCM_M10V	2	-10VDC Power	Out
Bx	3	Analog Voltage	In
N.C.	4	Y Shield	NC
By Return	5	Signal Return	In
Bz	6	Analog Voltage	In
CAL	7	+5V Digital Calibration Command signal	Out
N.C	8		NC
AGND	9	AGND	Out
Bx Return	10	Signal Return	In
N.C.	11	X Shield	NC
By	12	Analog Voltage	In
NC	13	Z Shield	NC
Bz Return	14	Signal Return	In
N.C.	15		NC

3.3. DCB interface

The DFB-DCB interface shall be through the backplane connector. The DFB shall transmit data to the DCB serially through the Data serial line—EFI_TLM. The DCB shall send commands to the DFB serially through the command serial line—EFI_CMD.

In addition the DCB shall transmit FGE data (FGE_TMH) to the DFB through a separate serial line. The interface for the FGE signal shall also be through the backplane.

The DCB shall transmit to the DFB a 1sec pulse (EFI_1HZ).

3.4. LVPS interface

The DFB shall interface to the LVPS through the backplane connector.

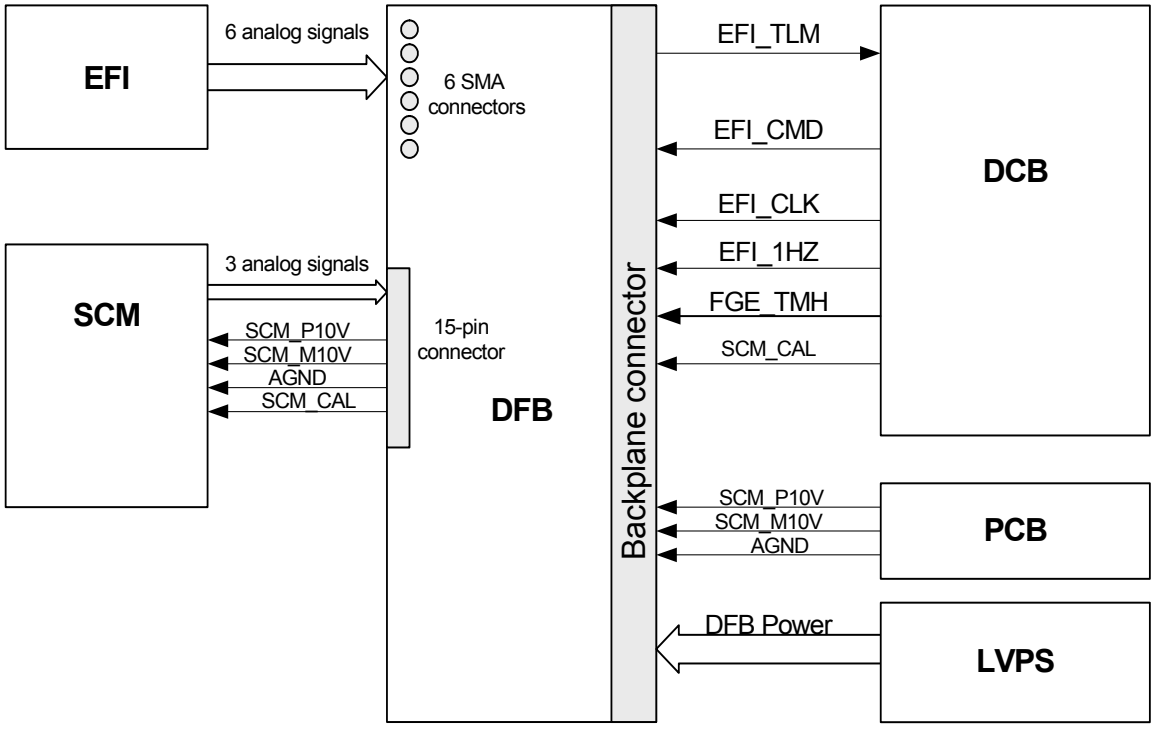


Figure 1: Interface and signal flow between DFB and other subsystem components.

4. Power

Power to the DFB shall be provided by the LVPS through the backplane connector. The DFB expects the following voltages:

+/- 10VDC Analog power <10mV ripple.
+/- 5VDC Analog power <10mV ripple.
+5VDC Digital power <50mV ripple.
+2.5VDC FPGA core power <50mV ripple.

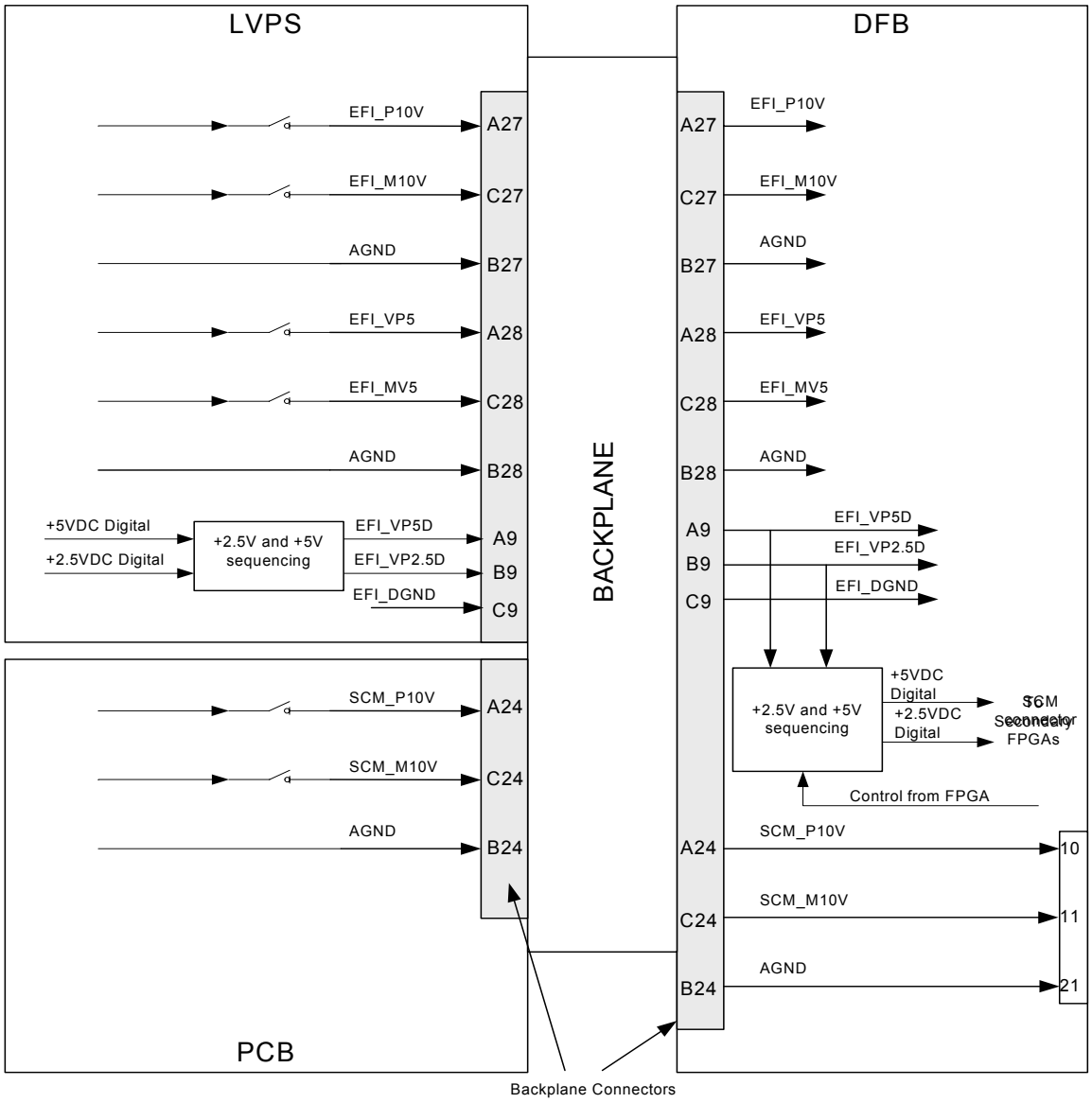


Figure 2: DFB and LVPS interface

All power provided to the DFB is switched on the LVPS. The LVPS shall also provide sequenced +5V digital and +2.5V—FPGA power. The sequencing shall be in compliance with the FPGA requirements as specified by the manufacturer. The sequencing of power to the secondary DFB FPGAs shall occur on the DFB. In addition, the PCB provides +/-10VDC to be routed through the DFB to the SCM.

5. DCB-DFB Serial interface circuit

The DFB and DCB communicate through a three wire serial interface. The wires are defined as follows:

1 wire for Command (CMD) data
1 wire for Telemetry (TLM) data
1 wire for 2^23Hz master clock (CLK)
1 wire for FGE data (FGE_TMH)
1 wire for the 1Hz pulse (EFI_1HZ)

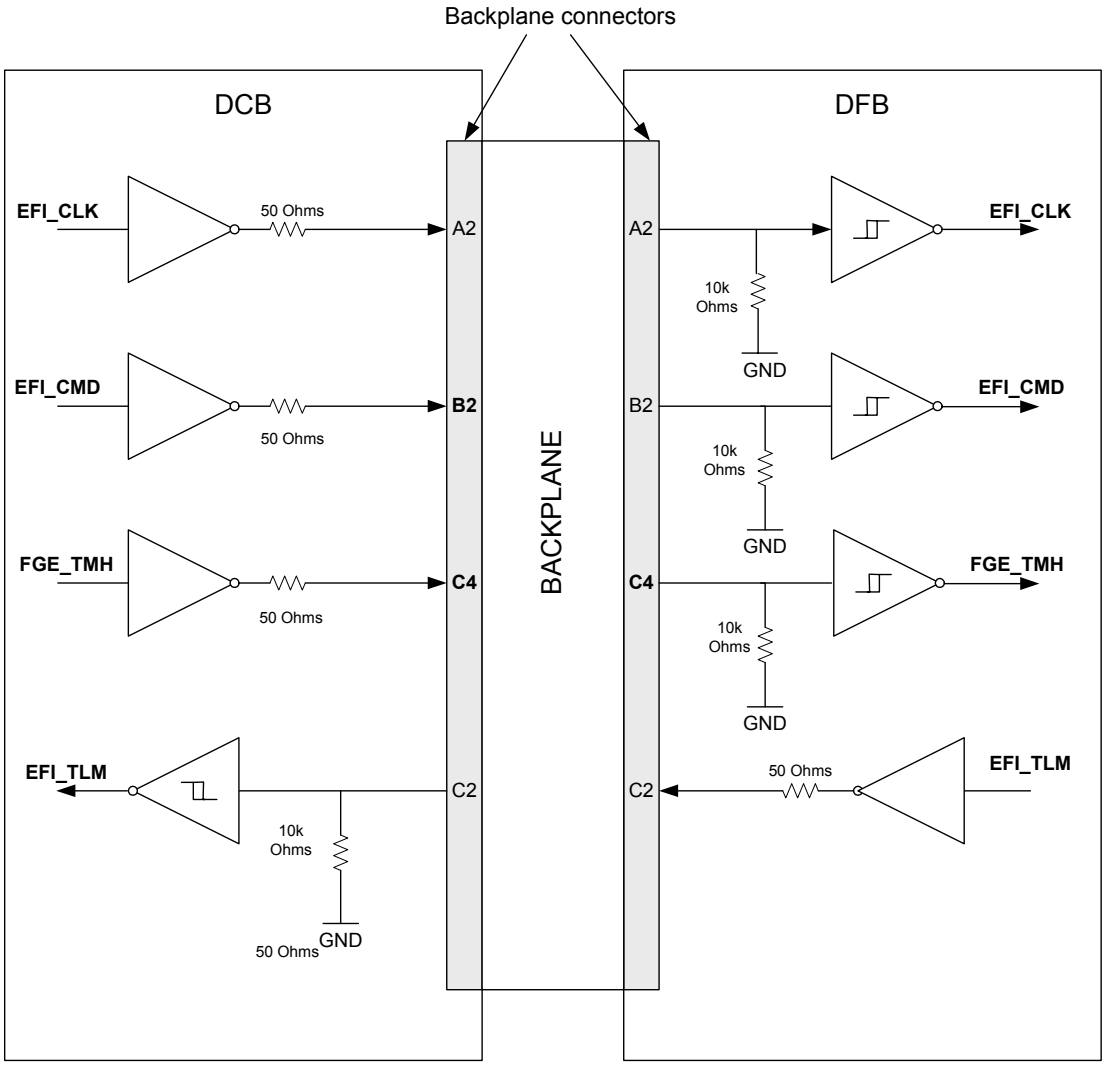


Figure 3: DFB-DCB serial interface

The EFI_CLK and EFI_CMD outputs from the DCB shall be maintained in such a state as to avoid partially powering the DFB FPGA when the DFB is off while the DCB is on.

6. Command and Telemetry Interface

6.1. Command (CMD)

The DCB transmits configuration commands to the DFB through the command serial line EFI_CMD. Commands from the DCB are 24-bits wide sent synchronously with the rising edge of the EFI_CLK. Eight bits are used for command identification (CMD_ID) and 16 bits are command information (CMD_DATA).

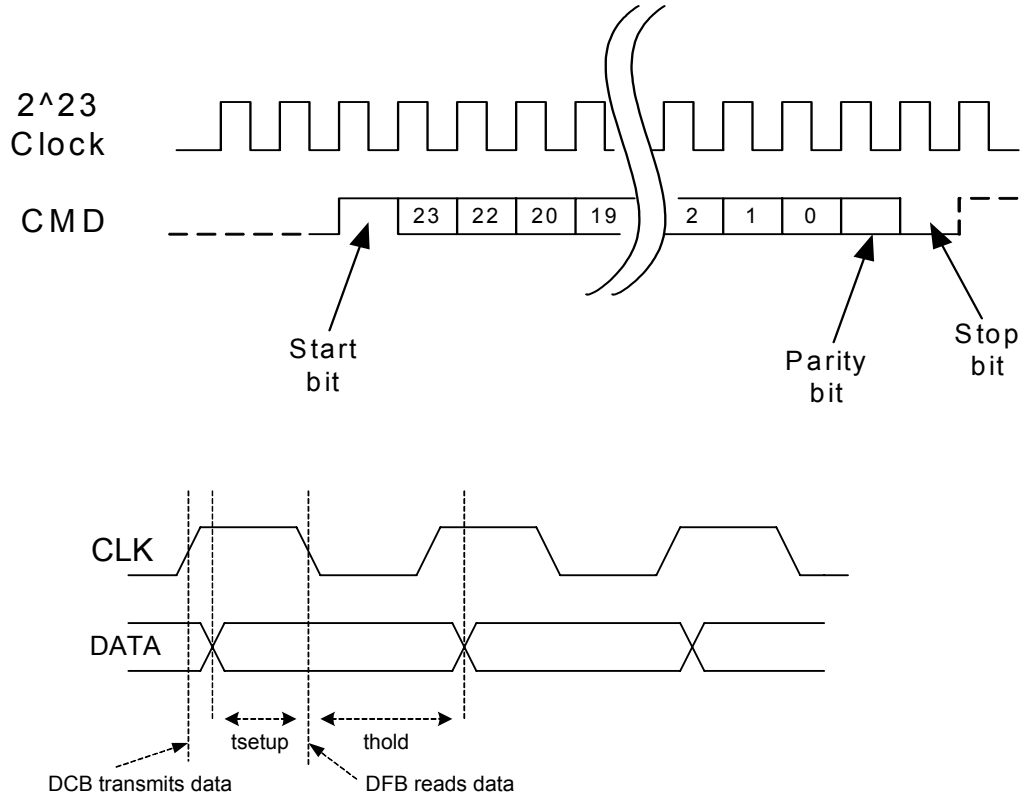


Figure 4: DFB Data Read Timing

tsetup = 30ns thold = 30ns
(referenced to the signals on the backplane)

The 24-bit commands are sent MSB first preceded by a start bit followed by a parity bit then by a stop bit. The parity is odd and includes the 24 command bits but not the start bit.

An enable command is sent by the DCB to enable Spin Fit and Trigger data.

No command retries will be attempted and no command echo by DFB is expected.

The DFB FPGA shall clock in the command data at the falling edge of CLK to avoid race conditions between EFI_CLK and EFI_CMD signals. Refer to appendix B for a list of DFB commands.

6.2. CMD Synchronization

The DFB synchronizes by finding the first non-zero bit (START bit), and verifies synchronization by the presence of a zero-value STOP bit. After a reset or loss of synchronization, the receiving system should look for 25 consecutive zero-level bits before starting to look for a start bit to avoid incorrect interpretation of a transfer in progress.

6.3. Telemetry (TLM)

DFB sends telemetry data as 24-bit words preceded by a start bit, followed by a parity bit and a stop bit. Parity is odd and includes the 24 data bits but not the start bit. EFI_TLM data shall be sent MSB first synchronously with the rising edge of the EFI_CLK. The DCB will shall sample the EFI_TLM data on the next rising edge of the clock.

The 24-bit word consists of 8-bits used for data identification (DATA_ID) and the remaining 16 bits is the value of the variable indicated by the DATA_ID. Refer to appendix A below for a list of DATA_ID and the corresponding variable.

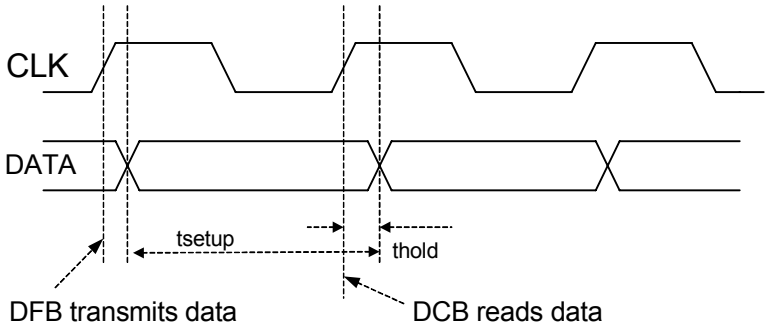


Figure 5: DFB Data Transmit Timing

tsetup = 30ns thold = 30ns

When commanded the DFB shall send housekeeping data consisting of (TBD) as a check of configuration validity and the correctness of various parameters (table) stored on the DFB. The housekeeping data is sent using ------- ID the same as Spin Fit data, which shall be disabled when housekeeping data is requested.
An enable/disable command is sent to the DFB by the DCB to request or disable Spin Fit, Filter Banks and HF data.

6.4. TLM Data Packet Rate

Telemetry data is transmitted by the DFB at various rates depending on operational modes and configurations. Maximum packet rate occurs in burst mode where up to 16 measurements at 16ksps could be transmitted by the DFB resulting in 256kwords/sec. Data from the DFB shall be transmitted on 1/32 second boundaries, synchronized to the 2^23 Hz (8MHz) system clock and the 1 second pulse. Data which are not available on every 1/32 second interval—such as spectra which are sent every 1/8 second—shall be synchronized to the 1/32 second transmission period such that they occur periodically by skipping the appropriate number of 1/32 second intervals.

6.5. TLM Synchronization

The DCB synchronizes by finding the first non-zero bit (START bit), in the EFI_TLM stream and verifies synchronization by the presence of a zero-value STOP bit. After a reset or loss of synchronization, the DCB should look for 25 consecutive zero-level bits before starting to look for a start bit to avoid incorrect interpretation of a transfer in progress. Further the DFB shall occasionally send 32 zero bits which the DCB could use for synchronization.

6.6. FGE DATA

The FGE data shall consist of six 16-bit words corresponding to the X,Y, and Z components of the magnetic field each being two 16-bit words—signed. The data shall be sent continuously at a rate of 128 Hz. A start bit shall precede each 16-bit word. No stop or parity bits are used. FGE data shall be used for cross-correlation with the EFI data sampled by the DFB.

A 1-second pulse sent by the DCB to both the FGE and DFB shall be used as the basis for synchronization between the DFB and EFI data. Time delays in propagating data with respect to the 1-second pulse shall therefore be known and fixed.

FGE Data shall follow the same rules as the command stream from the DCB in terms of clocking. Specifically, the DCB clocks out on the rising edge, and the DFB clocks in on the falling edge (with the point of reference being the backplane). *Note: all the CMD, TLM and CLK signals described in the Backplane Specification are specified in terms of how they appear on the backplane.*

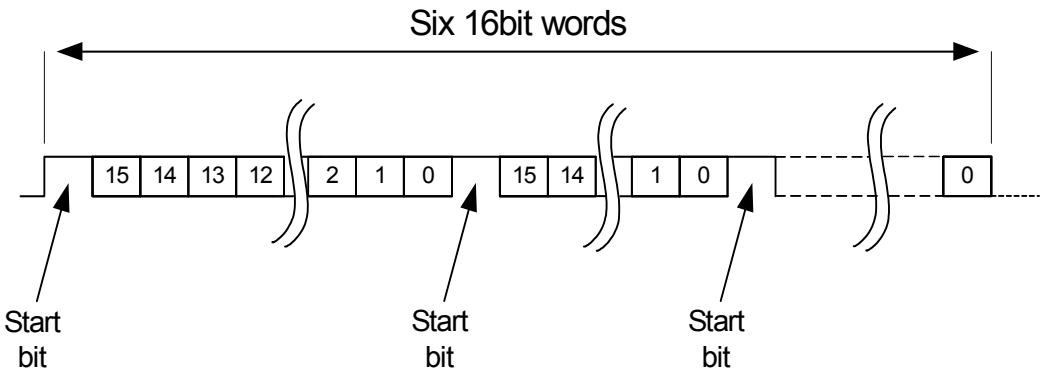


Figure 6: FGE Data Format

8. Appendix A – THEMIS DFB Command and Telemetry Information

DFB Commands

Command ID		Bit Definitions															
Decimal	Hex	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
64	0x40	-	FB_SPD[2:0]			-	-	-	-	FB2_SEL[3:0]				FB1_SEL[3:0]			
65	0x41	FS_VA_SPD[3:0]				-	-	-	-	-	-	FS_VA6_ENA	FS_VA5_ENA	FS_VA4_ENA	FS_VA3_ENA	FS_VA2_ENA	FS_VA1_ENA
66	0x42	FS_VB_SPD[3:0]				-	-	-	-	-	-	FS_VB6_ENA	FS_VB5_ENA	FS_VB4_ENA	FS_VB3_ENA	FS_VB2_ENA	FS_VB1_ENA
67	0x43	FS_E_SPD[3:0]				-	-	-	-	-	-	FS_E56AC_ENA	FS_E34AC_ENA	FS_E12AC_ENA	FS_E56DC_ENA	FS_E34DC_ENA	FS_E12DC_ENA
68	0x44	FS_SCM_SPD[3:0]				-	-	-	-	-	-	-	-	-	FS_SCM3_ENA	FS_SCM2_ENA	FS_SCM1_ENA
69	0x45	PB_VA_SPD[3:0]				-	-	-	-	-	-	PB_VA6_ENA	PB_VA5_ENA	PB_VA4_ENA	PB_VA3_ENA	PB_VA2_ENA	PB_VA1_ENA
70	0x46	PB_VB_SPD[3:0]				-	-	-	-	-	-	PB_VB6_ENA	PB_VB5_ENA	PB_VB4_ENA	PB_VB3_ENA	PB_VB2_ENA	PB_VB1_ENA
71	0x47	PB_E_SPD[3:0]				-	-	-	-	-	-	PB_E56AC_ENA	PB_E34AC_ENA	PB_E12AC_ENA	PB_E56DC_ENA	PB_E34DC_ENA	PB_E12DC_ENA
72	0x48	PB_SCM_SPD[3:0]				-	-	-	-	-	-	-	-	-	PB_SCM3_ENA	PB_SCM2_ENA	PB_SCM1_ENA
73	0x49	WB_VA_SPD[3:0]				-	-	-	-	-	-	WB_VA6_ENA	WB_VA5_ENA	WB_VA4_ENA	WB_VA3_ENA	WB_VA2_ENA	WB_VA1_ENA
74	0x4A	WB_VB_SPD[3:0]				-	-	-	-	-	-	WB_VB6_ENA	WB_VB5_ENA	WB_VB4_ENA	WB_VB3_ENA	WB_VB2_ENA	WB_VB1_ENA
75	0x4B	WB_E_SPD[3:0]				-	-	-	DER_E_ACDC	DER_EDOTB_ENA	DER_EXB_ENA	WB_E56AC_ENA	WB_E34AC_ENA	WB_E12AC_ENA	WB_E56DC_ENA	WB_E34DC_ENA	WB_E12DC_ENA
76	0x4C	WB_SCM_SPD[3:0]				-	-	-	-	DER_SCMDOTB_ENA	DER_SCMXB_ENA	-	-	-	WB_SCM3_ENA	WB_SCM2_ENA	WB_SCM1_ENA
77	0x4D	PB_SPEC_ENA	PB_SPEC_SPD[2:0]			PB_SPEC_NF[1:0]		SPEC2_SEL[4:0]					SPEC1_SEL[4:0]				
78	0x4E	WB_SPEC_ENA	WB_SPEC_SPD[2:0]			WB_SPEC_NF[1:0]		SPEC4_SEL[4:0]					SPEC3_SEL[4:0]				
79	0x4F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
80	0x50	-	-	-	-	-	-	-	ADC_SEL	ADC_MODE	WB_ENA	PB_ENA	FS_ENA	TR_MODE	TR_ENA	SS_ENA	GLOB_ENA
81	0x51	Placeholder/reminder for an upload command for derived quantities gain/offset uploads…format is TBD.															
82	0x52	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
83	0x53	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
84	0x54	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
85	0x55	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
86	0x56	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
87	0x57	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
88	0x58	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
89	0x59	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
90	0x5A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
91	0x5B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
92	0x5C	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
93	0x5D	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
94	0x5E	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
95	0x5F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Table A-1 - DFB Command Table

Filter Bank Configuration

Command ID #64: Filter Bank Configuration

Bit	Name	Description	Default
3:0	FB1_SEL[3:0]	Source selection for filter bank #1. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14 = E56AC, 15 = Undefined	6
7:4	FB2_SEL[3:0]	Source selection for filter bank #2. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14 = E56AC, 15 = Undefined	9
11:8	Undefined	-	0
14:12	FB_SPD[2:0]	Speed selection for filter banks. This controls how often the filter bank information in telemetry ID #64 is inserted into the telemetry stream. 0 = 1/16 S/s, 1 = 1/8 S/s, 2 = ¼ S/s, 3 = ½ S/s, 4 = 1 S/s, 5 = 2 S/s, 6 = 4 S/s, 7 = 8 S/s	2
15	Undefined	-	0

Fast Survey Configuration

Command ID #65: Fast Survey Filter Configuration – Voltage Group A

Bit	Name	Description	Default
0	FS_VA1_ENA	Fast-survey filter enable for V1. 1 = Enable, 0 = Disable	1
1	FS_VA2_ENA	Fast-survey filter enable for V2. 1 = Enable, 0 = Disable	1
2	FS_VA3_ENA	Fast-survey filter enable for V3. 1 = Enable, 0 = Disable	0
3	FS_VA4_ENA	Fast-survey filter enable for V4. 1 = Enable, 0 = Disable	0
4	FS_VA5_ENA	Fast-survey filter enable for V5. 1 = Enable, 0 = Disable	0
5	FS_VA6_ENA	Fast-survey filter enable for V6. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	FS_VA_SPD	Speed selection for fast-survey voltage group A. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	2

Command ID #66: Fast Survey Filter Configuration – Voltage Group B

Bit	Name	Description	Default
0	FS_VB1_ENA	Fast-survey filter enable for V1. 1 = Enable, 0 = Disable	0
1	FS_VB2_ENA	Fast-survey filter enable for V2. 1 = Enable, 0 = Disable	0
2	FS_VB3_ENA	Fast-survey filter enable for V3. 1 = Enable, 0 = Disable	0
3	FS_VB4_ENA	Fast-survey filter enable for V4. 1 = Enable, 0 = Disable	0
4	FS_VB5_ENA	Fast-survey filter enable for V5. 1 = Enable, 0 = Disable	0
5	FS_VB6_ENA	Fast-survey filter enable for V6. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	FS_VB_SPD	Speed selection for fast-survey voltage group B. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	0

Command ID #67: Fast Survey Filter Configuration – E

Bit	Name	Description	Default
0	FS_E12DC_ENA	Fast-survey filter enable for E12DC. 1 = Enable, 0 = Disable	1
1	FS_E34DC_ENA	Fast-survey filter enable for E34DC. 1 = Enable, 0 = Disable	1
2	FS_E56DC_ENA	Fast-survey filter enable for E56DC. 1 = Enable, 0 = Disable	1
3	FS_E12AC_ENA	Fast-survey filter enable for E12AC. 1 = Enable, 0 = Disable	0
4	FS_E34AC_ENA	Fast-survey filter enable for E34AC. 1 = Enable, 0 = Disable	0
5	FS_E56AC_ENA	Fast-survey filter enable for E56AC. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	FS_E_SPD	Speed selection for fast-survey E. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13 = 16384 S/s (data will only be valid in AC mode) 14-15 = Undefined	2

Command ID #68: Fast Survey Filter Configuration – SCM

Bit	Name	Description	Default
0	FS_SCM1_ENA	Fast-survey filter enable for SCM1. 1 = Enable, 0 = Disable	1
1	FS_SCM2_ENA	Fast-survey filter enable for SCM2. 1 = Enable, 0 = Disable	1
2	FS_SCM3_ENA	Fast-survey filter enable for SCM3. 1 = Enable, 0 = Disable	1
11:3	Undefined	-	0
15:12	FS_SCM_SPD	Speed selection for fast-survey SCM. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	2

Particle Burst Configuration

Command ID #69: Particle Burst Filter Configuration – Voltage Group A

Bit	Name	Description	Default
0	PB_VA1_ENA	Particle burst filter enable for V1. 1 = Enable, 0 = Disable	0
1	PB_VA2_ENA	Particle burst filter enable for V2. 1 = Enable, 0 = Disable	0
2	PB_VA3_ENA	Particle burst filter enable for V3. 1 = Enable, 0 = Disable	1
3	PB_VA4_ENA	Particle burst filter enable for V4. 1 = Enable, 0 = Disable	1
4	PB_VA5_ENA	Particle burst filter enable for V5. 1 = Enable, 0 = Disable	1
5	PB_VA6_ENA	Particle burst filter enable for V6. 1 = Enable, 0 = Disable	1
11:6	Undefined	-	0
15:12	PB_VA_SPD	Speed selection for particle burst voltage group A. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s 13-15 = Undefined	5

Command ID #70: Particle Burst Filter Configuration – Voltage Group B

Bit	Name	Description	Default
0	PB_VB1_ENA	Particle burst filter enable for V1. 1 = Enable, 0 = Disable	0
1	PB_VB2_ENA	Particle burst filter enable for V2. 1 = Enable, 0 = Disable	0
2	PB_VB3_ENA	Particle burst filter enable for V3. 1 = Enable, 0 = Disable	0
3	PB_VB4_ENA	Particle burst filter enable for V4. 1 = Enable, 0 = Disable	0
4	PB_VB5_ENA	Particle burst filter enable for V5. 1 = Enable, 0 = Disable	0
5	PB_VB6_ENA	Particle burst filter enable for V6. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	PB_VB_SPD	Speed selection for particle burst voltage group B. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s 13-15 = Undefined	0

Command ID #71: Particle Burst Filter Configuration – E

Bit	Name	Description	Default
0	PB_E12DC_ENA	Particle burst filter enable for E12DC. 1 = Enable, 0 = Disable	1
1	PB_E34DC_ENA	Particle burst filter enable for E34DC. 1 = Enable, 0 = Disable	1
2	PB_E56DC_ENA	Particle burst filter enable for E56DC. 1 = Enable, 0 = Disable	1
3	PB_E12AC_ENA	Particle burst filter enable for E12AC. 1 = Enable, 0 = Disable	0
4	PB_E34AC_ENA	Particle burst filter enable for E34AC. 1 = Enable, 0 = Disable	0
5	PB_E56AC_ENA	Particle burst filter enable for E56AC. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	PB_E_SPD	Speed selection for particle burst E. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13 = 16384 S/s (data will only be valid in AC mode) 14-15 = Undefined	6

Command ID #72: Particle Burst Filter Configuration – SCM

Bit	Name	Description	Default
0	PB_SCM1_ENA	Particle burst filter enable for SCM1. 1 = Enable, 0 = Disable	1
1	PB_SCM2_ENA	Particle burst filter enable for SCM2. 1 = Enable, 0 = Disable	1
2	PB_SCM3_ENA	Particle burst filter enable for SCM3. 1 = Enable, 0 = Disable	1
11:3	Undefined	-	0
15:12	PB_SCM_SPD	Speed selection for particle burst SCM. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s 13-15 = Undefined	6

Wave Burst Configuration

Command ID #73: Wave Burst Filter Configuration – Voltage Group A

Bit	Name	Description	Default
0	WB_VA1_ENA	Wave burst filter enable for V1. 1 = Enable, 0 = Disable	0
1	WB_VA2_ENA	Wave burst filter enable for V2. 1 = Enable, 0 = Disable	0
2	WB_VA3_ENA	Wave burst filter enable for V3. 1 = Enable, 0 = Disable	0
3	WB_VA4_ENA	Wave burst filter enable for V4. 1 = Enable, 0 = Disable	0
4	WB_VA5_ENA	Wave burst filter enable for V5. 1 = Enable, 0 = Disable	0
5	WB_VA6_ENA	Wave burst filter enable for V6. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	WB_VA_SPD	Speed selection for wave burst voltage group A. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	0

Command ID #74: Wave Burst Filter Configuration – Voltage Group B

Bit	Name	Description	Default
0	WB_VB1_ENA	Wave burst filter enable for V1. 1 = Enable, 0 = Disable	0
1	WB_VB2_ENA	Wave burst filter enable for V2. 1 = Enable, 0 = Disable	0
2	WB_VB3_ENA	Wave burst filter enable for V3. 1 = Enable, 0 = Disable	0
3	WB_VB4_ENA	Wave burst filter enable for V4. 1 = Enable, 0 = Disable	0
4	WB_VB5_ENA	Wave burst filter enable for V5. 1 = Enable, 0 = Disable	0
5	WB_VB6_ENA	Wave burst filter enable for V6. 1 = Enable, 0 = Disable	0
11:6	Undefined	-	0
15:12	WB_VB_SPD	Speed selection for wave burst voltage group B. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	0

Command ID #75: Wave Burst Filter Configuration – E

Bit	Name	Description	Default
0	WB_E12DC_ENA	Wave burst filter enable for E12DC. 1 = Enable, 0 = Disable	0
1	WB_E34DC_ENA	Wave burst filter enable for E34DC. 1 = Enable, 0 = Disable	0
2	WB_E56DC_ENA	Wave burst filter enable for E56DC. 1 = Enable, 0 = Disable	0
3	WB_E12AC_ENA	Wave burst filter enable for E12AC. 1 = Enable, 0 = Disable	0
4	WB_E34AC_ENA	Wave burst filter enable for E34AC. 1 = Enable, 0 = Disable	0
5	WB_E56AC_ENA	Wave burst filter enable for E56AC. 1 = Enable, 0 = Disable	0
6	DER_EXB_ENA	EXB download enable (for diagnostic purposes). Will only produce valid data when WB_E_SPD is set to highest valid rate based on the value of DER_E_ACDC. 1 = Enable, 0 = Disable	0
7	DER_EDOTB_ENA	EDOTB download enable (for diagnostic purposes). Will only produce valid data when WB_E_SPD is set to highest valid rate based on the value of DER_E_ACDC. 1 = Enable, 0 = Disable	0
8	DER_E_ACDC	Selects AC or DC coupled signals as the input to the derived quantity calculations for E. Note: this bit globally controls whether ExxDC or ExxAC values are used to create the derived quantities and so it effects the selection of input to the FFT as well. 1 = AC, 0 = DC	0
11:9	Undefined	-	0
15:12	WB_E_SPD	Speed selection for wave burst E. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13 = 16384 S/s (data will only be valid in AC mode), 14-15 = Undefined	0

Command ID #76: Wave Burst Filter Configuration – SCM

Bit	Name	Description	Default
0	WB_SCM1_ENA	Wave burst filter enable for SCM1. 1 = Enable, 0 = Disable	0
1	WB_SCM2_ENA	Wave burst filter enable for SCM2. 1 = Enable, 0 = Disable	0
2	WB_SCM3_ENA	Wave burst filter enable for SCM3. 1 = Enable, 0 = Disable	0
5:3	Undefined	-	0
6	DER_SCMXB_ENA	SCMXB download enable (for diagnostic purposes). Will only produce valid data when WB_SCM_SPD is set to highest rate. 1 = Enable, 0 = Disable	0
7	DER_SCMDOTB_ENA	SCMDOTB download enable (for diagnostic purposes). Will only produce valid data when WB_SCM_SPD is set to highest rate. 1 = Enable, 0 = Disable	0
11:8	Undefined	-	0
15:12	WB_SCM_SPD	Speed selection for wave burst SCM. 0 = 2 S/s, 1 = 4 S/s, 2 = 8 S/s, 3 = 16 S/s, 4 = 32 S/s, 5 = 64 S/s, 6 = 128 S/s, 7 = 256 S/s, 8 = 512 S/s, 9 = 1024 S/s, 10 = 2048 S/s, 11 = 4096 S/s, 12 = 8192 S/s, 13-15 = Undefined	0

Spectra Configuration

Command ID #77: Particle Burst Spectra Configuration

Bit	Name	Description	Default
4:0	SPEC1_SEL[4:0]	Source selection for FFT processor #1. This controls the source for both the particle burst and the wave burst spectral analysis. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14, E56AC, 15 = Undefined, 16 = EXB, 17 = EDOTB, 18 = SCMXB, 19 = SCMDOTB, 20-31 = Undefined	0
9:5	SPEC2_SEL[4:0]	Source selection for FFT processor #2. This controls the source for both the particle burst and the wave burst spectral analysis. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14, E56AC, 15 = Undefined, 16 = EXB, 17 = EDOTB, 18 = SCMXB, 19 = SCMDOTB, 20-31 = Undefined	0
11:10	PB_SPEC_NF[1:0]	Selects the number of frequency bins in the particle burst spectral data inserted into the telemetry stream. 0 = 16 bins, 1 = 32 bins, 2 = 64 bins, 3 = Undefined	0
14:12	PB_SPEC_SPD[2:0]	Speed selection for particle burst spectra. This controls how often the particle burst spectral information in telemetry ID #77 is inserted into the telemetry stream. 0 = 1/16 S/s, 1 = 1/8 S/s, 2 = ¼ S/s, 3 = ½ S/s, 4 = 1 S/s, 5 = 2 S/s, 6 = 4 S/s, 7 = 8 S/s	0
15	PB_SPEC_ENA	Particle burst spectra enable. Controls all 4 particle burst FFT processors. 1 = Enable, 0 = Disable	0

Command ID #78: Wave Burst Spectra Configuration

Bit	Name	Description	Default
4:0	SPEC3_SEL[4:0]	Source selection for FFT processor #3. This controls the source for both the particle burst and the wave burst spectral analysis. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14, E56AC, 15 = Undefined, 16 = EXB, 17 = EDOTB, 18 = SCMXB, 19 = SCMDOTB, 20-31 = Undefined	0
9:5	SPEC4_SEL[4:0]	Source selection for FFT processor #4. This controls the source for both the particle burst and the wave burst spectral analysis. 0 = V1, 1 = V2, 2 = V3, 3 = V4, 4 = V5, 5 = V6, 6 = E12DC, 7 = E34DC, 8 = E56DC, 9 = SCM1, 10 = SCM2, 11 = SCM3, 12 = E12AC, 13 = E34AC, 14, E56AC, 15 = Undefined, 16 = EXB, 17 = EDOTB, 18 = SCMXB, 19 = SCMDOTB, 20-31 = Undefined	0
11:10	WB_SPEC_NF[1:0]	Selects the number of frequency bins in the wave burst spectral data inserted into the telemetry stream. 0 = 16 bins, 1 = 32 bins, 2 = 64 bins, 3 = Undefined	0
14:12	WB_SPEC_SPD[2:0]	Speed selection for wave burst spectra. This controls how often the particle burst spectral information in telemetry ID #78 is inserted into the telemetry stream. 0 = 1/16 S/s, 1 = 1/8 S/s, 2 = ¼ S/s, 3 = ½ S/s, 4 = 1 S/s, 5 = 2 S/s, 6 = 4 S/s, 7 = 8 S/s	0
15	WB_SPEC_ENA	Wave burst spectra enable. Controls all 4 wave burst FFT processors. 1 = Enable, 0 = Disable	0

Global Configuration

Command ID #80: Global Configuration

Bit	Name	Description	Default
0	GLOB_ENA	Global telemetry enable. This bit globally enables the transfer of telemetry data from the DFB to the DCB. This bit can be set or reset at any time via software command to start/stop telemetry. On power-up, this bit will automatically be set to "1" after 16 seconds to enable the default configuration. Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	1
1	SS_ENA	Slow-survey telemetry enable. This bit enables the transfer of telemetry data from the DFB to the DCB for the slow-survey quantities (data for spin-fit, filter banks, and HF processing). Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	1
2	TR_ENA	Trigger telemetry enable. This bit enables the transfer of telemetry data from the DFB to the DCB for the trigger quantities or the housekeeping data depending on the value of TR_MODE. Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	1
3	TR_MODE	Trigger telemetry mode. This bit selects whether trigger or housekeeping data is transmitted on data ID 81. 1 = Housekeeping, 0 = Trigger	0
4	FS_ENA	Fast-survey telemetry enable. This bit enables the transfer of telemetry data from the DFB to the DCB for the fast-survey quantities (fast-survey filters). Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	1
5	PB_ENA	Particle burst telemetry enable. This bit enables the transfer of telemetry data from the DFB to the DCB for the particle burst quantities (particle burst filters and particle burst spectral information). Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	1
6	WB_ENA	Wave burst telemetry enable. This bit enables the transfer of telemetry data from the DFB to the DCB for the wave burst quantities (wave burst filters and wave burst spectral information). Changes in state are implemented on the next one-second boundary. 1 = Enable, 0 = Disable	0
7	ADC_MODE	Selects the ADC mode. Normal mode shares the acquisition load among the two ADCs (8kS/s to ADC #1 and 16kS/s to ADC #2) in order to maximize settling time. Backup mode uses	0

		a single ADC (indicated by ADC_SEL) for all acquisitions. 1 = Backup, 0 = Normal	
8	ADC_SEL	Selects the active ADC in backup mode. 1 = ADC #2, 0 = ADC #1	0
15:9	Undefined		

DFB Telemetry

Name	Data ID	Ap ID	Type	Global Enable	ADC Source	For	Fmin (Hz)	Fmax (Hz)	# Components		Rate (S/s)			Bits	Rate (bits/s)		Duty Cycle	Vol. to DCB (24 hr)	Telemetry (24 hr)
									Range	Typical	Min	Typical	Max		Typical	Max			
Spin Fit Quantities																			**3.23 M**
VFit	80	--	SpinFit	SS_ENA	V1-V4	DCB Proc	DC	50	4	4	128	128	128	16	8192	8192	100%	707.79 M	0.46 M
EFit	80	--	SpinFit	SS_ENA	E12DC, E34DC, E56DC	DCB Proc	DC	50	3	3	128	128	128	16	6144	6144	100%	530.84 M	2.76 M
Trigger Data / Housekeeping																			
FBankT1	81	--	Trig	TR_ENA	Same as Fbank1	DCB Proc.	1.6	3 kHz	11	11	16	16	16	8	1408	1408	100%	12165 M	
FBankT2	81	--	Trig	TR_ENA	Same as Fbank2	DCB Proc.	1.6	3 kHz	11	11	16	16	16	8	1408	1408	100%	12165 M	
HFPeakT	81	--	Trig	TR_ENA	HF	DCB Proc.	100k	500k	1	1	16	16	16	8	128	128	100%	1106 M	
HFAveT	81	--	Trig	TR_ENA	HF	DCB Proc.	100k	500k	1	1	16	16	16	8	128	128	100%	1106 M	
HK	81	--	HK	TR_ENA	None	Diagnostic	--	--	64?	64?	64?	--	64?	16	--	1024?	--		
Filter Bank / Slow Survey																			**2.42 M**
FBank1	64	64	SS	SS_ENA	Any ADC Source	DCB SSTM	0.8	3 kHz	6	6	1/16	1/4	8	8	12	384	100%	104 M	104 M
FBank2	64	64	SS	SS_ENA	Any ADC Source	DCB SSTM	0.8	3 kHz	6	6	1/16	1/4	8	8	12	384	100%	104 M	104 M
HFPeak	64	64	SS	SS_ENA	HF	DCB SSTM	100k	500k	1	1	1/16	1/4	8	8	2	64	100%	0.17 M	0.17 M
HFAve	64	64	SS	SS_ENA	HF	DCB SSTM	100k	500k	1	1	1/16	1/4	8	8	2	64	100%	0.17 M	0.17 M
Fast Survey Waveforms																			**16.17 M**
VAFS	65	65	FS	FS_ENA	V1-V6	DCB FSTM	DC	0.8-100	0-6	2	2	2	256	16	64	24 k	45%	2.49 M	1.24 M
VBFS	66	66	FS	FS_ENA	V1-V6	DCB FSTM	DC	0.8-100	0-6	0	2	--	256	16	--	24 k	45%		
EFS	67	67	FS	FS_ENA	E12, 34, 56 DC/AC	DCB FSTM	DC	0.8-100	0-3	3	2	8	256	16	384	12 k	45%	14.93 M	7.46 M
SCMFS	68	68	FS	FS_ENA	SCM1, SCM2, SCM3	DCB FSTM	1Hz	0.8-100	0-3	3	2	8	256	16	384	12 k	45%	14.93 M	7.46 M
Particle Burst Waveforms																			**27.65 M**
VAPB	69	69	PB	PB_ENA	V1-V6	DCB FSTM	DC	0.8-100	0-6	2	2	16	256	16	512	24 k	5%	2.21M	1.11M
VBPB	70	70	PB	PB_ENA	V1-V6	DCB FSTM	DC	0.8-100	0-6	0	2	--	256	16	--	24 k	5%		
EPB	71	71	PB	PB_ENA	E12, 34, 56 DC/AC	DCB FSTM	DC	0.8-100	0-3	3	2	128	256	16	6144	12 k	5%	26.54 M	13.27 M
SCMPB	72	72	PB	PB_ENA	SCM1, SCM2, SCM3	DCB FSTM	1Hz	0.8-100	0-3	3	2	128	256	16	6144	12 k	5%	26.54 M	13.27 M
Wave Burst Waveforms																			**19.82 M**
VAWB	73	73	WB	WB_ENA	V1-V6	DCB FSTM	DC	200-3k	0-6	1	512	8192	8192	16	128 k	768 k	0.05%	5.66 M	2.83 M
VBWB	74	74	WB	WB_ENA	V1-V6	DCB FSTM	DC	200-3k	0-6	0	512	--	8192	16	--	768 k	0.05%		
EWB	75	75	WB	WB_ENA	E12, 34, 56 DC/AC	DCB FSTM	DC	200-6k	0-3	3	512	8192	16384	16	384 k	768 k	0.05%	16.99 M	8.49 M
SCMWB	76	76	WB	WB_ENA	SCM1, SCM2, SCM3	DCB FSTM	1Hz	200-3k	0-3	3	512	8192	8192	16	384 k	384 k	0.05%	16.99 M	8.49 M
EDER	75	75	DER	WB_ENA	Derived	Diagnostic	DC	6k/12k	0-2	0	8k/16k	--	8k/16k	16	--	512 k	0.05%		
SCMDER	76	76	DER	WB_ENA	Derived	Diagnostic	1Hz	6k	0-2	0	8192	--	8192	16	--	256 k	0.05%		
Particle Burst Spectra																			**4.42 M**
Spec1	77	77	PB	PB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	32	1/4	1	8	8	256	4096	5%	1.11M	1.11M
Spec2	77	77	PB	PB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	32	1/4	1	8	8	256	4096	5%	1.11M	1.11M
Spec3	77	77	PB	PB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	32	1/4	1	8	8	256	4096	5%	1.11M	1.11M
Spec4	77	77	PB	PB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	32	1/4	1	8	8	256	4096	5%	1.11M	1.11M
Wave Burst Spectra																			**0.71 M**
Spec1	78	78	WB	WB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	64	1/4	8	8	8	4096	4096	0.05%	0.18 M	0.18 M
Spec2	78	78	WB	WB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	64	1/4	8	8	8	4096	4096	0.05%	0.18 M	0.18 M
Spec3	78	78	WB	WB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	64	1/4	8	8	8	4096	4096	0.05%	0.18 M	0.18 M
Spec4	78	78	WB	WB_ENA	ADC or Derived	DCB FSTM	8	8k	16, 32, 64	64	1/4	8	8	8	4096	4096	0.05%	0.18 M	0.18 M

Table A-2 - DFB Telemetry Table

The available DFB telemetry values are summarized in Table A-2. The transmission synchronization and formatting are illustrated in Figure A-1. The following important points are depicted by the telemetry data format diagram:

- Data transmission occurs in discrete 31.25 ms windows that are aligned with the 1 second pulse from the DCB.
- Data is played out sequentially in the order that it is listed in Table A-2 (except for the housekeeping which is sent last) where the sequence within a line item is determined according to the order of the enable bits in the command listing in section 0.
- Samples from individual quantities are transferred in "block" format (an example of V1 is shown in Figure A-1) before moving on to the next quantity in order to simplify the FPGA logic and to enhance data compression by grouping like data as close together as possible.
- The maximum data transfer length is TBD. This will also give us a value for the guaranteed idle time before the next time-slot begins.

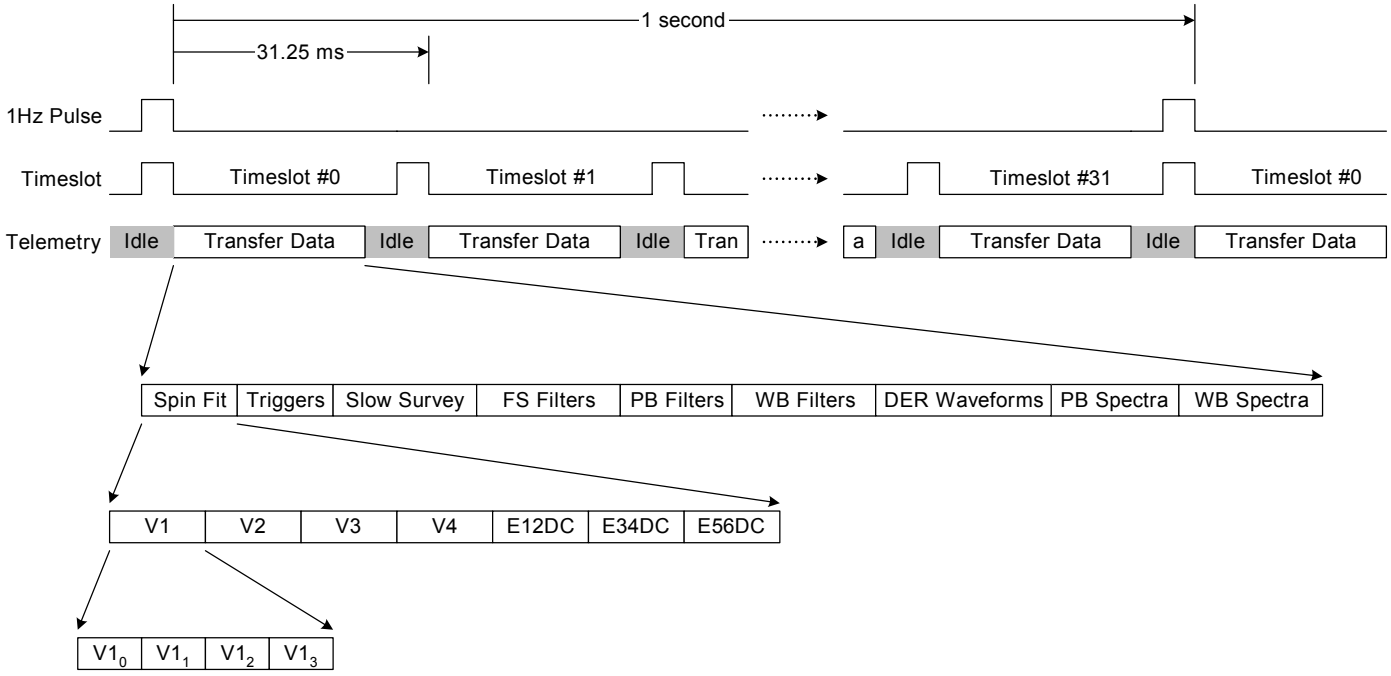


Figure A-1 - DFB Telemetry Data Format

9. Appendix B

Backplane connector pin assignment

Pin #	Signal Name	Signal Function	LVPS	FGE PCB	DCB	BEB	DFB
A1	DGND	Digital Ground					
B1	DGND	Digital Ground					
C1	DGND	Digital Ground					
A2	EFI CLK	EFI Clock Input			S	R	R
B2	EFI CMD	EFI Command Input			S	R	R
C2	EFI TLM	EFI Telemetry Output			R		S
A3	EFI 1Hz	EFI Sync 1Hz			S		R
C5	FGE TMHB	Buffered FGE TLM			S		R
A9	EFI_VP5D	+5V Digital		S		R	R
B9	EFI_VP2.5D	+2.5V Digital		S		R	R
C9	EFI_DGND	Digital Ground		S		R	R
A24	SCM_P10V	SCM +10V		S			R
B24	AGND			S			R
C24	SCM_M10V	SCM +10V		S			R
A25	SCM_CAL	SCM Calibration			S		R
A27	EFI _P10V	EFI +10V	S			R	R
B27	AGND		S			R	R
C27	EFI _M10V	EFI -10V	S			R	R
A28	EFI_VP5	EFI +5V	S				R
B28	AGND		S				R
C28	EFI_VM5	EFI -5V	S				R

10. Appendix C